AMENDMENTS TO THE SPECIFICATION

Please amend lines 8-15 of p. 2 of the Specification as follows:

One aspect of processor performance relates to monitoring certain addresses such as instruction addresses via, for example, a watchpoint address or a sample address range. When monitoring the instruction address, it becomes important to quickly compare the instruction address against the watchpoint address or the sample address range. ~~What~~ When a match is detected between the instruction address and the monitoring address, the processor takes some sort of action such as generating a watchpoint trap if the address matches the watchpoint address or collecting sampling information if the instruction address is within the sample address range.

Please amend lines 11-20 of p. 6 of the Specification as follows:

The instruction fetch unit 110 is responsible for fetching instructions from the instruction cache and then sending the resulting bundles of instructions to the instruction renaming unit 112. The instruction fetch unit may fetch up to eight instructions per cycle. Each group of ~~instruction s~~ instructions delivered to by the instruction fetch unit is referred to as a fetch bundle. The instruction cache sources instructions to the processor pipeline by accessing a local instruction cache with predetermined cache indices. The instruction is virtually addressed by an instruction pointer generator. The branch prediction logic enables the instruction fetch unit 110 to speculatively fetch ~~instruction s~~ instructions beyond a control transfer instruction (CTI) even though the outcome or target of the control transfer instruction is not yet known.

Please amend lines 21-26 of p. 6 of the Specification as follows:

The instruction renaming unit 112 decodes instructions, determines instruction dependencies and manages certain processor resources. The instruction scheduling unit 114 ~~scheduling~~ schedules instructions from each thread for execution, replays instructions that are consumers of loads when the load misses in the data cache, maintains completion and trap status for instructions executing within the processor 100 and separately retires ~~instruction sin~~ instructions in fetch order from each thread.

Please amend lines 3-5 of p. 7 of the Specification as follows:

The memory management unit 130 performs virtual address to physical address translation and includes a translation lookaside buffer that provides ~~fro~~ for a translation for the most frequently accessed virtual pages.

Please amend lines 7-14 of p. 9 of the Specification as follows:

The data TLB supports access ~~permission s~~ permissions for data accesses, while the memory management unit supports instruction accesses. The memory management unit supports access to a translation storage buffer, which is a direct mapped structure in memory which holds memory mappings as translation table entries. The memory management unit may either directly query the translation storage buffer via hardware or may generate a trap which allows software to query the translation storage buffer and then write the mapping into the memory management unit when an access causes the memory management unit ~~misses~~ to miss on a mapping.

Please amend lines 21-27 of p. 10 of the Specification as follows:

FIG. 5 shows a block diagram of a micro translation look aside buffer entry. More specifically, each entry of the instruction TLB includes a mapping from the upper bits of the Virtual Address to the upper bits of the Physical Address. Each entry of the instruction TLB also includes a partial address compare field for the entry. The partial address compare field includes eight bits that represent the partial compare of the upper bits of the Virtual Address to a virtual address watchpoint trap address ~~as well~~ as well as bits that represent whether the address is within a sample address range.